NANO LETTERS

pubs.acs.org/NanoLett

Letter

CMOS-Compatible Protonic Programmable Resistor Based on Phosphosilicate Glass Electrolyte for Analog Deep Learning

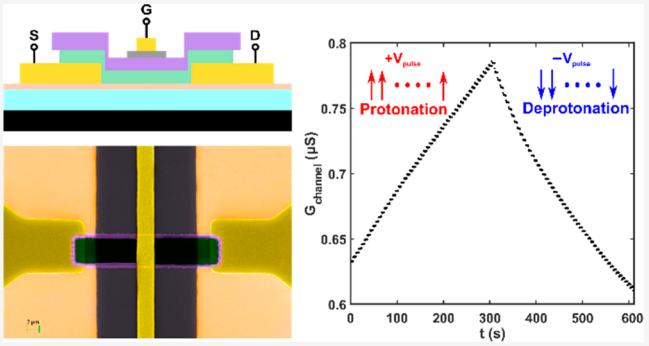
Murat Onen, Nicolas Emond, Ju Li,* Bilge Yildiz,* and Jesús A. del Alamo*

Cite This: *Nano Lett.* 2021, 21, 6111−6116

Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

ABSTRACT: Ion intercalation based programmable resistors have emerged as a potential next-generation technology for analog deep-learning applications. Proton, being the smallest ion, is a very promising candidate to enable devices with high modulation speed, low energy consumption, and enhanced endurance. In this work, we report on the first back-end CMOS-compatible nonvolatile protonic programmable resistor enabled by the integration of phosphosilicate glass (PSG) as the proton solid electrolyte layer. PSG is an outstanding solid electrolyte material that displays both excellent protonic conduction and electronic insulation characteristics. Moreover, it is a well-known material within conventional Si fabrication, which enables precise deposition control and scalability. Our scaled all-solid-state three-terminal devices show desirable modulation characteristics in terms of symmetry, retention, endurance, and energy efficiency. Protonic programmable resistors based on phosphosilicate glass, therefore, represent promising candidates to realize nanoscale analog crossbar processors for monolithic CMOS integration.



KEYWORDS: *analog computing, doped silicon dioxide films, proton intercalation, programmable resistors*

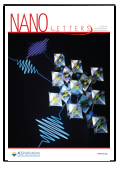
1. INTRODUCTION

The success of deep learning in classifying and clustering representations of data at multiple levels of abstraction has fundamentally changed how information is processed.[1] However, conventional digital architectures face increasing difficulties in supporting the heavy computational workloads required to train state of the art deep neural networks (DNNs).[2] The pressing need for faster and more energy-efficient deep-learning processors has therefore led to an intensive investigation of in-memory computation schemes using analog crossbar arrays.[3,4]

The basic building block of analog crossbar arrays is the crosspoint element, which can be described as a programmable, nonvolatile resistor.[5] For a DNN to be trained successfully (i.e., without degradation of classification performance) with such architectures, the resistive devices need to have many nonvolatile conductance states that can be modulated reversibly, symmetrically, and reproducibly.[3,6] A plethora of device technologies has been proposed for analog deep learning applications such as phase-change memories,[7] filamentary[8] and bulk-switching[9] resistive memories, ferroelectric tunnel junctions,[10] spintronics,[11] and superconducting nanowires.[12] Despite significant advances in the aforementioned fields, no device technology has been identified so far that meets all of the requirements.[3]

Recently, a novel device family relying on electrochemically controlled ion intercalation in transition-metal oxide channels (also referred to as electrochemical random access memory, ECRAM) has shown promising characteristics.[13−19] Due to their similarities to solid-state batteries, the most mature versions of these devices rely on shuffling Li^+ ions across a Li^+-conducting electron-insulating electrolyte, metered by electron flow in the outer metallic circuit.[13−15] Approaches based on alkali-metal ions (Li^+, Na^+, K^+, Ca^{2+}) suffer from CMOS incompatibility, due to contamination concerns of the fabrication tools. Proton (H^+) intercalation devices are thus considered to have the edge in realizing scalable programmable resistors that are back-end-of-line (BEOL) integrable.[17−19] Moreover, the smallest ionic radius of protons (Shannon−Prewitt effective ionic radius of −0.18 Å if 2-fold coordinated and −0.38 Å if one-fold coordinated) promises high modulation speed, low energy consumption, and enhanced endurance. Indeed, in our recent work,[18] we demonstrated promising device characteristics using a PdH_x solid hydrogen

Received: April 23, 2021
Revised: June 29, 2021
Published: July 7, 2021



https://doi.org/10.1021/acs.nanolett.1c01614
Nano Lett. 2021, 21, 6111−6116

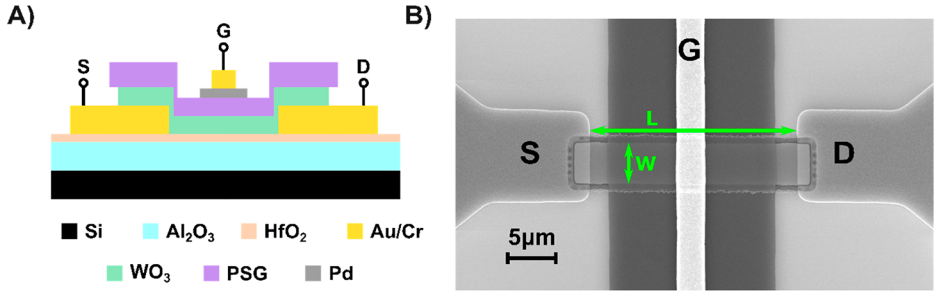


Figure 1. (A) Schematic of the protonic programmable resistor studied in this work. (B) Top-view scanning electron microscope image of a finished device showing the source (S), drain (D), and gate (G) of a device with a nominal channel width (W) of 5 μm and a length (L) of 25 μm.

reservoir, polymeric Nafion electrolyte, and WO_3 channel material for proton intercalation.

However, the main bottleneck with developing protonic programmable resistors has been the absence of a CMOS-compatible all-solid-state electrolyte that conducts protons but blocks electrons. All designs so far have relied on approaches that either cannot be integrated and scaled down, such as using organic materials,[17] using chemically and thermally sensitive polymers (e.g. Nafion),[18] or suffer from energy inefficiency such as high electric-field-induced water hydrolysis.[19] Furthermore, some protonic electrolytes rely on water absorption for proton conduction, requiring repeated rehydration of the material during operation.[20]

In this work, we demonstrate a CMOS-compatible protonic programmable resistor based on a nanoporous phosphosilicate glass (PSG) solid electrolyte. PSG is an excellent choice for this application due to its (1) good electronic insulation, (2) high room-temperature proton conductivity, (3) conduction mechanism based on P doping (instead of structural water), and (4) ready availability in conventional Si processing. The selection of this material has allowed us to use standard CMOS-fabrication techniques and consequently scale down the device footprint. Our devices show desirable modulation characteristics in terms of symmetry, retention, endurance, and energy efficiency. This new device technology appears promising in the quest to satisfy the stringent performance requirements for analog crosspoint elements. Furthermore, PSG enables exploration of alternative channel and hydrogen reservoir layers, while using a fully CMOS compatible and scalable fabrication platform.

2. DEVICE OPERATION

The protonic programmable resistor demonstrated in this work is a three-terminal device that employs a WO_3 channel, a PSG electrolyte layer, and a Pd gate reservoir (Figure 1A). We adopt a transistor-like notation to refer to the three terminals of this device. The terms "source" and "drain" are used to refer to the two ends of the WO_3 channel, while the term "gate" is used to refer to the PdH_x proton reservoir.

The basic operation principle of the device relies on modulating the channel conductance via the electrochemically controlled intercalation of protons into WO_3, as explained in our recent work.[18] Initially, protons are stored in the gate reservoir as PdH_x, which is achieved by the hydrogen uptake of Pd in a forming gas ambient (3% H_2 in N_2).[21] With the application of a voltage pulse, a controlled number of protons are moved from the gate to the channel through the solid electrolyte, while electrons concurrently move through the external circuit in the same direction. This process can be reversed by the application of a voltage pulse of inverse polarity, forcing protons out of the channel back into the gate reservoir. Protons are n-type dopants in WO_3,[22] and as they move in and out, the conductivity of the channel is modulated up and down. Furthermore, in the absence of a programming pulse (i.e., floating gate), proton motion toward either the gate or the channel is precluded, as the electrolyte prevents the electron flow required to satisfy charge neutrality in the channel and reservoir layers. This last feature establishes nonvolatility with the channel conductance remaining constant at its last programmed level.

Among several oxides whose electronic conductivity can be tuned via cation intercalation (WO_3,[18] V_2O_5,[23] MoO_3,[24] Nb_2O_5[25]), we chose to use amorphous tungsten oxide (a-WO_3) as the channel material. This selection was motivated by the well-established conductivity modulation[13,16,18] and electrochromism[19] dynamics with cation intercalation. a-WO_3 is a CMOS-compatible semiconductor with a band gap of 2.8–3.2 eV whose conductivity can be precisely modulated by protonation, taking place concurrently with charge-balancing electron filling of the W 5d orbital dominated conduction band in the dilute regime. The structure of a-WO_3 at room temperature is assumed to be similar to that of its crystalline counterpart (monoclinic based on corner-sharing WO_6 octahedra), but with disordered bond lengths and angles. The most common defect present in the WO_3 lattice structure is an oxygen vacancy, which bonds to a W^{6+} ion, reduces the oxidation state of the neighboring W^{5+} ion, and increases the conductivity, in a way analogous to the way the electron does with proton intercalation (see Figure S1). The extent of conductivity modulation in a-WO_3 by proton intercalation, therefore, depends on its initial defect concentration that determines its initial conductivity.[26]

In the search for an inorganic CMOS-compatible electrolyte layer, we focused on silicate glasses (SiO_2), which are widely used in Si technology as electron insulators.[27] Deposition conditions of silicate glasses can be engineered to yield a nanoporous structure with defect −OH terminated Si groups (silanol), providing a surface-site path for ion transport along the pores.[28] The acidic nature of silanol acts as a proton donor, which then migrates by hopping between hydroxyl groups and structural water.[29,30] Doping silicate glasses with phosphorus sterically hinders the glass network to increase nonbridging oxygen bonds,[31] replaces Si−O−Si bonds with −Si−OH and −Si−O−P−OH groups, and increases both the pore volume and surface area.[32] The P−OH groups not only have higher acidity in comparison to silanol but are also amphoteric, meaning that they can act as both proton donors and acceptors.[33] These are all key properties that provide

https://doi.org/10.1021/acs.nanolett.1c01614
Nano Lett. 2021, 21, 6111−6116

phosphosilicate glass (PSG, P-SiO_2) high proton conductivity at room temperature (2.54×10^{-4} S cm^{-1}), which stands among the highest values in comparison with several perovskite, fluorite, and simple oxide proton-conducting materials,[34] while retaining their electron-insulating properties.[35] Furthermore, even though the proton conductivity of PSG can be further increased to 10^{-1} S cm^{-1} by an additional hydrothermal treatment[36] and chemisorption of water in the pore structure,[37] such modifications also result in an increased electronic conductivity of the material, which is undesirable for our design that requires nonvolatile throttling of hydrogen in WO_3.

3. METHODS

The protonic programmable resistors were fabricated on a Si substrate covered with 10/90 nm HfO_2/Al_2O_3 deposited by atomic layer deposition (ALD) for electrical and protonic insulation. Channel contacts (15/5 nm Au/Cr) were first patterned using a direct-write photolithography and liftoff process. A 10 nm WO_3 channel and 10 nm PSG electrolyte layers were blanket-deposited using ALD and plasma-enhanced chemical vapor deposition (PECVD) processes, respectively. The deposition conditions for PSG (T = 100 °C, 60 W plasma power, and gas flow ratio of 12 sccm SiH_4/12 sccm PH_3 diluted at 2% in H_2) were found to be optimal to maximize proton conductivity, as reported in ref 35. The PSG/WO_3 stack was subsequently patterned with a self-aligned reactive ion etching (RIE) process, followed by TMAH-based wet etching of WO_3 to create a PSG overhang that prevents shorting of the channel with the gate at the edges of the device. Different channel dimensions (i.e., width and length) were patterned in the range between 2 and 100 μm. Finally, the 5 nm Pd reservoir and 150/10 nm Au/Cr gate interconnect and pads were electron beam evaporated and patterned through separate liftoff processes. A cross-sectional view of a finished device is shown in Figure 1A. Full details of the fabrication process can be found in Figure S2 in the Supporting Information. Figure 1B shows the top-view scanning electron microscope image of a fabricated structure. Given the standard Si-fabrication compatibility of this process flow, it can easily be adapted to yield nanoscale devices by replacing the photolithography steps with their electron-beam lithography versions.

An atomic force microscopy (AFM) image of a PSG film deposited under the optimum conditions on a Si substrate is shown in Figure 2A. A nanogranular structure (so-called nanoglass) with a mean glassy grain diameter of ~80 nm and an RMS roughness of ~1 nm is observed. This image also evidences the presence of nanopores with a high surface to volume ratio, an essential requirement for efficient proton transport in this material.

The stoichiometric ratio of each element in the optimized PSG film (PSG 12:12) was found to be 0.55% P, 45.65% Si, and 53.8% O using X-ray photoelectron spectroscopy (XPS). The spectra of undoped (SiO_2), optimized (PSG 12:12), and more highly doped (PSG 12:24) films, deposited with 12:0, 12:12 and 12:24 SiH_4:PH_3 flux, respectively, were acquired (Figure 2B). While the intensity of the P 2p peak, located at a binding energy of ~134 eV (inset), increases with PH_3 flux, that of the Si 2p peak decreases. The estimated P concentration of the PSG 12:12 film is 0.55%, a value similar to those reported for PSG films with optimized proton conductivity (2.5×10^{-4} S cm^{-1}).[35]

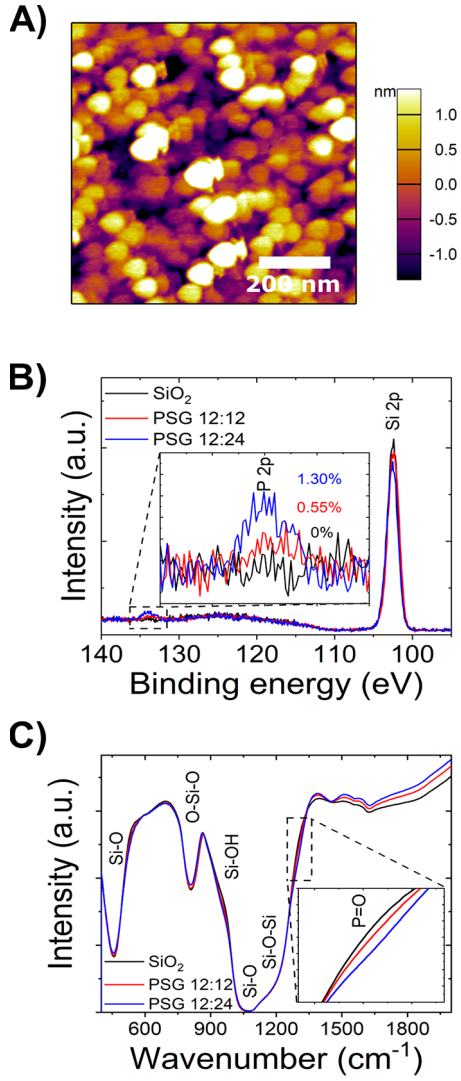


Figure 2. (A) Atomic force microscopy image of the PSG 12:12 thin film surface deposited on a Si surface. (B) X-ray photoelectron spectra of the P 2p and Si 2p peaks and (C) Fourier transform infrared spectra of the SiO_2, PSG 12:12, and PSG 12:24 thin films. The inset in (B) shows enlarged spectra in the P 2p energy range, while the inset in (C) shows enlarged spectra in the P═O absorption region.

The presence of P in the films was also confirmed by Fourier transform infrared spectroscopy (FTIR). As shown in Figure 2C, the increase in PH_3 flux results in the appearance of P═O and Si−OH absorption bands around 1300 cm^{-1} (inset) and 1130 cm^{-1}, respectively, as well as a decrease in the intensity of the Si−O and Si−O−Si bands. All of these features are indicative of the successful incorporation of P atoms in the glass structure.

4. RESULTS

Electrical characterization of the devices was conducted at room temperature in an enclosed probe station (NEXTRON MPS-PT) filled with forming gas (3% H_2 in N_2, see the Supporting Information for further details). The basic modulation properties of the devices were first measured to assess their conductance modulation depth, symmetry, retention, and endurance (Figure 3) in a pulsing mode. Figure 3A shows the increase in conductance upon the application of 100 positive voltage pulses (increment, red, V_G = 3 V, 1 s) and

https://doi.org/10.1021/acs.nanolett.1c01614
Nano Lett. 2021, 21, 6111−6116

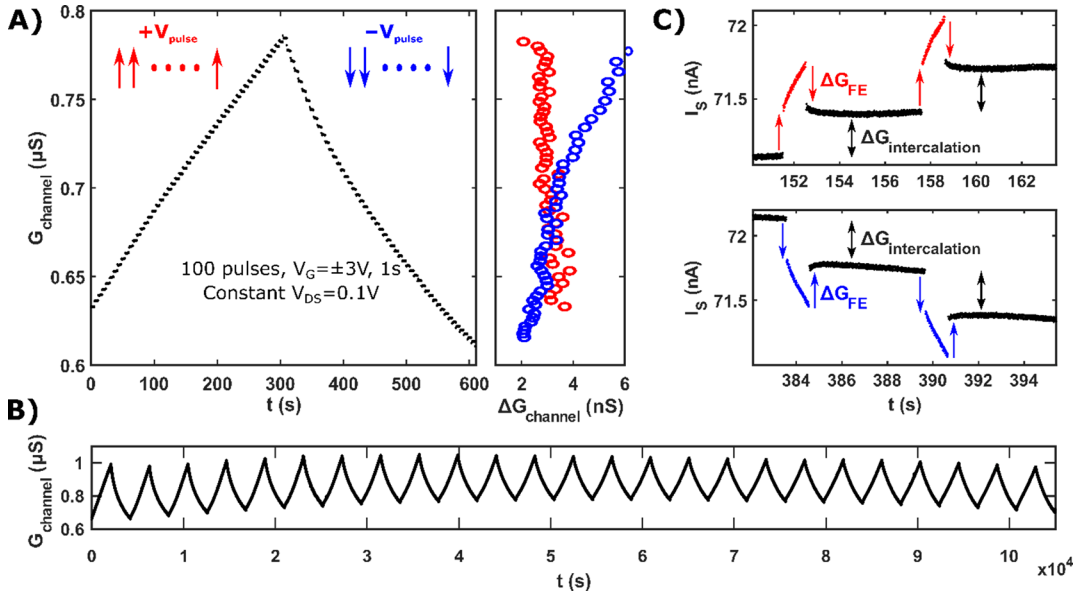


Figure 3. (A) (left) Modulation characteristics of a protonic programmable resistor (5 μm width, 50 μm length) determined by applying 50 voltage pulses of ±3 V and 1 s width in either direction. Each state is monitored for 2 s by measuring the channel current while V_{DS} = 0.1 V is applied. (right) Conductance change ($\Delta G_{channel}$) plotted at different conductance levels ($G_{channel}$). Incremental changes are shown with red markers, while decremental changes are shown with blue markers. (B) Endurance characterization throughout the application of 50000 voltage pulses (25 × [1000 ↑ 1000 ↓]) of ±3 V and 0.1 s width over the course of ∼30 h. (C) Detailed picture of (A) where the channel current, I_S, is constantly recorded in the presence (colored dots) and absence (dark dots) of gate pulses.

decrease upon that of 100 negative pulses (decrement, blue, V_G = 3 V, 1 s). V_{DS} was constantly maintained at 0.1 V throughout the update sequence.

Figure 3A demonstrates very clean device conductance modulation characteristics with high symmetry and non-volatility of the programmed conductance, due to the electron-blocking properties of the PSG thin-film electrolyte (see Figure S3). A well-defined symmetry point (i.e., a conductance level at which the incremental change is equal to the decremental change in conductance) is also evidenced, as well as excellent cycling endurance characteristics, with very little variation in conductance values even after the application of 50000 pulses over the course of ∼30 h (Figure 3B). Furthermore, we did not observe any noticeable open-circuit voltage development across the gate stack, allowing the operation under constant voltage pulses.

It should be noted that the base (i.e., unprotonated) conductance of the channel material is significantly higher than that of stoichiometric WO_3, therefore limiting the conductance modulation depth and the speed of the channel upon proton intercalation.[18,26] Such behavior is expected on consideration of the oxygen-deficient nature of the ALD-deposited WO_3. Indeed, an XPS analysis (Figure S6) clearly evidences a large degree of initial tungsten reduction (W^{5+}:W^{6+} ratio) and in-gap states present in the film. To mitigate this issue, the deposition method of WO_3 can be modified to target the optimal stoichiometry or alternative channel materials (e.g., V_2O_5, MoO_3, Nb_2O_5) can be used as a replacement.

A careful analysis of the modulation dynamics (Figure 3C) unravels interesting device physics, comprised of both volatile and nonvolatile changes in conductance, as programming pulses are applied. Under constant V_{DS} = 0.1 V, the source current, I_S, immediately steps up/down when a gate pulse (±3 V) is applied and then smoothly increases/decreases for the remainder of the pulse duration (colored dots). Once the pulse disappears (i.e., floating gate), another sudden drop/rise in I_S is observed. In the absence of a gate pulse, I_S remains approximately constant, at a level different from that before the application of the pulse, indicating nonvolatile programming of the channel conductance (dark dots). These sudden changes in I_S do not reflect an increase in gate current, I_G (<pA), but are due to a field-effect enhancement of the channel conductance (ΔG_{FE}). This behavior can be explained by a field-effect increase in the electron concentration and a resulting increase in conductance of the n-type WO_3 channel by the electrostatic field of protons driven within the electrolyte close to the WO_3 interface.[38,39] Unlike the nonvolatile, electrochemical intercalation induced conductance modulation ($\Delta G_{intercalation}$), this additional channel current only flows during the application of a gate voltage pulse and therefore it is volatile.

The initial channel conductance and average modulation magnitude of protonic crosspoint elements for 20 devices with varying dimensions were also examined. Figure 4A shows that both parameters scale linearly with the channel width/length (W/L) ratio, as expected. This well-behaved scaling demonstrates both a promising yield and uniformity for these PSG-based devices.

Using different channel dimensions, we have also estimated the energy efficiency and its scaling for protonic programmable resistors presented in this work. As the figure of merit, we chose the ratio of energy consumption required to change the channel conductance by a small amount ($E/\Delta G_{channel}$). This choice also enables us to compare the same value with those reported for O^{2-} ion intercalation devices in ref 16. Figure 4B reveals that, at the same device area of 200 μm^2, our devices consume 0.45 mJ/S, which is 1000× more energy efficient with respect to its heavier-ion alternative. Considering that this metric scales with L^2 (not area), we estimate the pulse energy required for a single state increment of a 100 × 100 nm^2

https://doi.org/10.1021/acs.nanolett.1c01614
Nano Lett. 2021, 21, 6111−6116

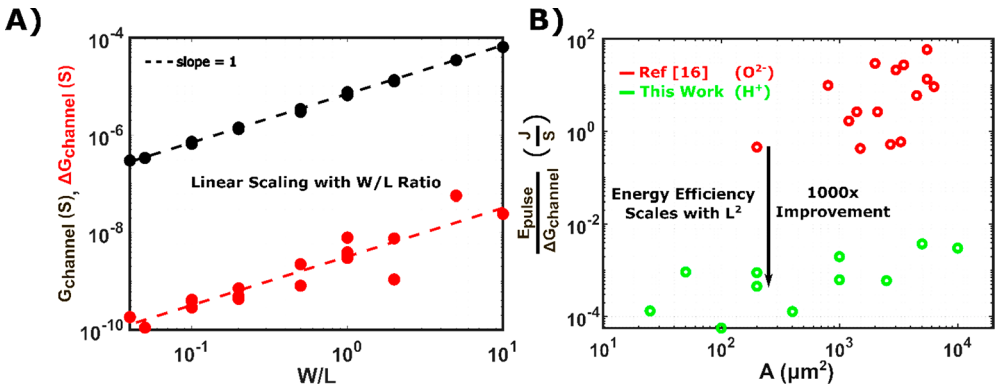


Figure 4. (A) Scaling of conductance and average conductance modulation magnitude for different channel geometries (W/L). (B) Comparison of device energy efficiency with respect to other CMOS-compatible oxygen ion intercalation devices reported in ref 16.

protonic device would be ∼1 fJ, assuming a conductance range of 1−10 MΩ modulated with 1 nS incremental changes (i.e., 900 states). We expect this number to further improve upon the implementation of a stoichiometric WO_3 channel, since the oxygen-deficient nature of the current material limits its overall modulation amplitude ($\Delta G_{channel}$), as explained earlier.

5. CONCLUSION

In this work, we demonstrated a back-end CMOS-compatible protonic programmable resistor that can serve as a crosspoint element in analog crossbar processors. Conductance modulation, device scalability, and process control are ensured by the use of a thin nanoporous PSG layer, a common and CMOS-compatible material, as the proton electrolyte layer. Our devices, which also include a WO_3 channel and a PdH_x reservoir, display low energy consumption along with symmetric and nonvolatile conductance modulation for an extended number of voltage pulses. Downscaling of the device dimensions, using electron-beam lithography or other techniques, as well as the possibility of BEOL integration to CMOS chips, can be also envisioned for our technology. Ultimately, PSG can serve as a platform to explore alternative channel and hydrogen reservoir layers in protonic programmable resistors, which present desirable characteristics to realize next-generation analog accelerators for deep-learning applications.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.1c01614.

Details of fabrication, characterization methods, additional results, and discussions (PDF)

■ AUTHOR INFORMATION

Corresponding Authors

Ju Li − *MIT-IBM Watson AI Lab, Cambridge, Massachusetts 02142, United States; Department of Materials Science and Engineering and Department of Nuclear Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, United States;* orcid.org/0000-0002-7841-8058; Email: liju@mit.edu

Bilge Yildiz − *MIT-IBM Watson AI Lab, Cambridge, Massachusetts 02142, United States; Department of Materials Science and Engineering and Department of Nuclear Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, United States;* orcid.org/0000-0002-2688-5666; Email: byildiz@mit.edu

Jesús A. del Alamo − *Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, United States; MIT-IBM Watson AI Lab, Cambridge, Massachusetts 02142, United States;* Email: alamo@mit.edu

Authors

Murat Onen − *Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, United States; MIT-IBM Watson AI Lab, Cambridge, Massachusetts 02142, United States;* orcid.org/0000-0002-9078-2901

Nicolas Emond − *MIT-IBM Watson AI Lab, Cambridge, Massachusetts 02142, United States; Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, United States*

Complete contact information is available at: https://pubs.acs.org/10.1021/acs.nanolett.1c01614

Funding

This project was funded by MIT-IBM Watson AI Research Lab. N.E. thanks the "Fonds de recherche du Québec et Nature et technologies (FRQNT)" for financial support.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

We thank John Rozen, Teodor Todorov, and Paul Solomon from IBM T. J. Watson Research Center for program support and fruitful discussions. We thank Dongha Kim for performing the XPS measurements. Device fabrication has taken place at the facilities of MIT.nano and the MIT Electron-Beam Lithography Facility at MIT. Materials characterization took place at the facilities of the MIT Materials Research Laboratory.

■ REFERENCES

(1) Lecun, Y.; Bengio, Y.; Hinton, G. Deep learning. *Nature* **2015**, *521*, 436−444.

(2) Strubell, E.; Ganesh, A.; McCallum, A. Energy and policy considerations for deep learning in NLP. *ACL 2019 - 57th Annu. Meet. Assoc. Comput. Linguist. Proc. Conf.* **2019**, 3645−3650.

(3) Gokmen, T.; Vlasov, Y. Acceleration of Deep Neural Network Training with Resistive Cross-Point Devices: Design Considerations. *Front. Neurosci.* **2016**, *10*, 333.
(4) Cai, F.; Correll, J. M.; Lee, S. H.; Lim, Y.; Bothra, V.; Zhang, Z.; Flynn, M. P.; Lu, W. D. A fully integrated reprogrammable memristor-CMOS system for efficient multiply-accumulate operations. *Nat. Electron.* **2019**, *2*, 290.
(5) Steinbuch, K. Die Lernmatrix. *Kybernetik.* **1961**, *1*, 36−45.
(6) Agarwal, S.; Plimpton, S. J.; Hughart, D. R.; Hsia, A. H.; Richter, I.; Cox, J. A.; James, C. D.; Marinella, M. J. Resistive memory device requirements for a neural algorithm accelerator. *Proc. Int. Jt. Conf. Neural Networks* **2016**, 929−938.
(7) Burr, G. W.; Shelby, R. M.; Sidler, S.; Di Nolfo, C.; Jang, J.; Boybat, I.; Shenoy, R. S.; Narayanan, P.; Virwani, K.; Giacometti, E. U.; Kurdi, B. N.; Hwang, H. Experimental Demonstration and Tolerancing of a Large-Scale Neural Network (165 000 Synapses) Using Phase-Change Memory as the Synaptic Weight Element. *IEEE Trans. Electron Devices* **2015**, *62*, 3498−3507.
(8) Jiang, H.; Han, L.; Lin, P.; Wang, Z.; Jang, M. H.; Wu, Q.; Barnell, M.; Yang, J. J.; Xin, H. L.; Xia, Q. Sub-10 nm Ta Channel Responsible for Superior Performance of a HfO2Memristor. *Sci. Rep.* **2016**, *6*, 28525.
(9) Li, Y.; Fuller, E. J.; Sugar, J. D.; Yoo, S.; Ashby, D. S.; Bennett, C. H.; Horton, R. D.; Bartsch, M. S.; Marinella, M. J.; Lu, W. D.; Talin, A. A. Filament-Free Bulk Resistive Memory Enables Deterministic Analogue Switching. *Adv. Mater.* **2020**, *32*, 2003984.
(10) Chanthbouala, A.; Garcia, V.; Cherifi, R. O.; Bouzehouane, K.; Fusil, S.; Moya, X.; Xavier, S.; Yamada, H.; Deranlot, C.; Mathur, N. D.; Bibes, M.; Barthélémy, A.; Grollier, J. A ferroelectric memristor. *Nat. Mater.* **2012**, *11*, 860−864.
(11) Grollier, J.; Querlioz, D.; Camsari, K. Y.; Everschor-Sitte, K.; Fukami, S.; Stiles, M. D. Neuromorphic spintronics. *Nat. Electron.* **2020**, *3*, 360−370.
(12) Onen, M.; Butters, B. A; Toomey, E.; Gokmen, T.; Berggren, K. K Design and characterization of superconducting nanowire-based processors for acceleration of deep neural network training. *Nanotechnology* **2020**, *31*, 025204.
(13) Tang, J.; Bishop, D.; Kim, S.; Copel, M.; Gokmen, T.; Todorov, T.; Shin, S.; Lee, K. T; Solomon, P.; Chan, K.; Haensch, W.; Rozen, J. ECRAM as Scalable Synaptic Cell for High-Speed, Low-Power Neuromorphic Computing. In *Technical Digest - International Electron Devices Meeting, IEDM*; IEEE: 2018; pp 13.1.1−13.1.4.
(14) Fuller, E. J.; El Gabaly, F.; Léonard, F.; Agarwal, S.; Plimpton, S. J.; Jacobs-Gedrim, R. B.; James, C. D.; Marinella, M. J.; Talin, A. A. Li-Ion Synaptic Transistor for Low Power Analog Computing. *Adv. Mater.* **2017**, *29*, 1604310.
(15) Zhu, J.; Yang, Y.; Jia, R.; Liang, Z.; Zhu, W.; Rehman, Z. U.; Bao, L.; Zhang, X.; Cai, Y.; Song, L.; Huang, R. Ion Gated Synaptic Transistors Based on 2D van der Waals Crystals with Tunable Diffusive Dynamics. *Adv. Mater.* **2018**, *30*, 1800195.
(16) Kim, S.; Todorov, T.; Onen, M.; Gokmen, T.; Bishop, D.; Solomon, P.; Lee, K.; Copel, M.; Farmer, D. B.; Ott, J. A.; Ando, T.; Miyazoe, H.; Narayanan, V.; Rozen, J. Metal-oxide based, CMOS-compatible ECRAM for Deep Learning Accelerator. *IEEE Int. Electron Devices Meet.* **2019**, 35.7.1.
(17) Van De Burgt, Y.; Lubberman, E.; Fuller, E. J.; Keene, S. T.; Faria, G. C.; Agarwal, S.; Marinella, M. J.; Alec Talin, A.; Salleo, A. A non-volatile organic electrochemical device as a low-voltage artificial synapse for neuromorphic computing. *Nat. Mater.* **2017**, *16*, 414−418.
(18) Yao, X.; Klyukin, K.; Lu, W.; Onen, M.; Ryu, S.; Kim, D.; Emond, N.; Waluyo, I.; Hunt, A.; del Alamo, J. A.; Li, J.; Yildiz, B. Protonic solid-state electrochemical synapse for physical neural networks. *Nat. Commun.* **2020**, *11*, 1−10.
(19) Katase, T.; Onozato, T.; Hirono, M.; Mizuno, T.; Ohta, H. A transparent electrochromic metal-insulator switching device with three-terminal transistor geometry. *Sci. Rep.* **2016**, *6*, 1−9.
(20) Liu, L.; Chen, W.; Li, Y. An overview of the proton conductivity of nafion membranes through a statistical analysis. *J. Membr. Sci.* **2016**, *504*, 1−9.
(21) Li, Y.; Cheng, Y. T. Hydrogen diffusion and solubility in palladium thin films. *Int. J. Hydrogen Energy* **1996**, *21*, 281−291.
(22) Powell, A. W.; Stavrinadis, A.; Christodoulou, S.; Quidant, R.; Konstantatos, G. On-Demand Activation of Photochromic Nano-heaters for High Color Purity 3D Printing. *Nano Lett.* **2020**, *20*, 3485−3491.
(23) Kulish, V. V.; Manzhos, S. Comparison of Li, Na, Mg and Al-ion insertion in vanadium pentoxides and vanadium dioxides. *RSC Adv.* **2017**, *7*, 18643−18649.
(24) Sen Yang, C.; Shang, D. S.; Liu, N.; Shi, G.; Shen, X.; Yu, R. C.; Li, Y. Q.; Sun, Y. A Synaptic Transistor based on Quasi-2D Molybdenum Oxide. *Adv. Mater.* **2017**, *29*, 1−10.
(25) Orel, B.; Maček, M.; Grdadolnik, J.; Meden, A. In situ UV-Vis and ex situ IR spectroelectrochemical investigations of amorphous and crystalline electrochromic Nb2O5 films in charged/discharged states. *J. Solid State Electrochem.* **1998**, *2*, 221−236.
(26) Niklasson, G. A.; Granqvist, C. G. Electrochromics for smart windows: Thin films of tungsten oxide and nickel oxide, and devices based on these. *J. Mater. Chem.* **2007**, *17*, 127−156.
(27) Sassella, A.; Borghesi, A.; Rojas, S.; Zanotti, L. Optical Properties of CVD-Deposited Dielectric Films for Microelectronic Devices. *J. Phys. IV* **1995**, *05*, C5-843−C5-859.
(28) Moore, C. W.; Li, J.; Kohl, P. A. Microfabricated fuel cells with thin-film silicon dioxide proton exchange membranes. *J. Electrochem. Soc.* **2005**, *152*, A1606.
(29) Colomer, M. T.; Jurado, J. R. Proton Conductivity in Nanopore Silica Xerogels. *Ionics* **2003**, *9*, 207−213.
(30) Chapple-Sokol, J. D.; Pliskin, W. A.; Conti, R. A.; Tierney, E.; Batey, J. Energy Considerations in the Deposition of High-Quality Plasma-Enhanced CVD Silicon Dioxide. *J. Electrochem. Soc.* **1991**, *138*, 3723−3726.
(31) Abe, Y.; Hosono, H.; Ohta, Y.; Hench, L. L. Protonic conduction in oxide glasses: Simple relations between electrical conductivity, activation energy, and the o-h bonding state. *Phys. Rev. B: Condens. Matter Mater. Phys.* **1988**, *38*, 10166−10169.
(32) Nogami, M.; Nagao, R.; Wong, C.; Kasuga, T.; Hayakawa, T. High Proton Conductivity in Porous P2O5-SiO2 Glasses. *J. Phys. Chem. B* **1999**, *103*, 9468−9472.
(33) Jiang, S. P. Functionalized mesoporous structured inorganic materials as high temperature proton exchange membranes for fuel cells. *J. Mater. Chem. A* **2014**, *2*, 7637−7655.
(34) Meng, Y.; Gao, J.; Zhao, Z.; Amoroso, J.; Tong, J.; Brinkman, K. S. Review: recent progress in low-temperature proton-conducting ceramics. *J. Mater. Sci.* **2019**, *54*, 9291−9312.
(35) Prakash, S.; Mustain, W. E.; Park, S. H.; Kohl, P. A. Phosphorus-doped glass proton exchange membranes for low temperature direct methanol fuel cells. *J. Power Sources* **2008**, *175*, 91−97.
(36) Li, H.; Jin, D.; Kong, X.; Tu, H.; Yu, Q.; Jiang, F. High proton-conducting monolithic phosphosilicate glass membranes. *Microporous Mesoporous Mater.* **2011**, *138*, 63−67.
(37) Nogami, M.; Tarutani, Y.; Daiko, Y.; Izuhara, S.; Nakao, T.; Kasuga, T. Preparation of P[sub 2]O[sub 5]-SiO[sub 2] Glasses with Proton Conductivity of ∼ 100 mS/cm at Room Temperature. *J. Electrochem. Soc.* **2004**, *151*, A2095.
(38) Vanheusden, K.; Warren, W. L.; Devine, R. A. B.; Fleetwood, D. M.; Draper, B. L.; Schwank, J. R. Non-volatile MOSFET memory device based on mobile protons in SiO2 thin films. *J. Non-Cryst. Solids* **1999**, *254*, 1−10.
(39) Liu, N.; Zhu, L. Q.; Xiao, H.; Wan, C. J.; Liu, Y. H.; Chao, J. Y. Transient characteristics for proton gating in laterally coupled indium-zinc-oxide transistors. *ACS Appl. Mater. Interfaces* **2015**, *7*, 6205−6210.

https://doi.org/10.1021/acs.nanolett.1c01614
Nano Lett. 2021, 21, 6111−6116

Supplementary Materials for CMOS-compatible Protonic Programmable Resistor based on Phosphosilicate Glass Electrolyte for Analog Deep Learning

Authors: Murat Onen[1,2], Nicolas Emond [2,3], Ju Li [2,3,4,*], Bilge Yildiz [2,3,4,*], Jesús A. del Alamo [1,2,*]

Affiliations:

1 Microsystems Technology Laboratories, Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, MA 02139, USA

2 MIT-IBM Watson AI Lab, 75 Binney St, Cambridge, MA 02142, USA

3 Department of Materials Science and Engineering, Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, MA 02139, USA

4 Department of Nuclear Science and Engineering, Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, MA 02139, USA

*Corresponding Authors: alamo@mit.edu, byildiz@mit.edu, liju@mit.edu

1. Device Operation

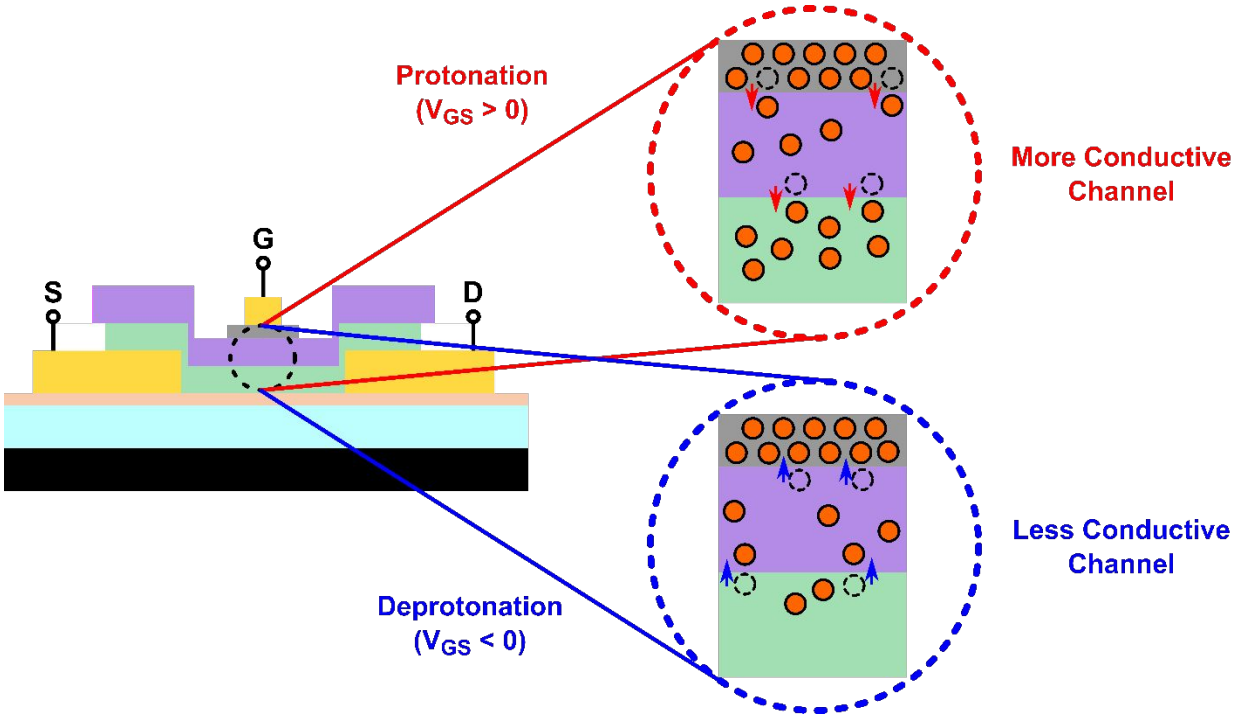


Figure S1. Operational illustration of CMOS-compatible protonic nonvolatile resistors studied in this work.

2. Fabrication Flow

- Atomic Layer Deposition (ALD) of 90 nm Al_2O_3 (for proton blocking properties) and 10 nm HfO_2 (to protect Al_2O_3 from TMAH and CF_4 plasma) on an undoped 4" Si wafer for electronic and protonic insulation.
- Spin-coating of Polymethylglutarimide (PMGI) at 4 krpm for 60 s (thickness $\approx$ 120 nm) and baking at 180°C for 90 s. Spin-coating of Microposit S1813 positive tone photoresist at 4 krpm for 60 s (thickness $\approx$ 1.8 **μ**m) and baking at 100°C for 90 s.
- Exposition of the source and drain electrode (M1) layout using a Heidelberg maskless aligner (MLA) 150 with a 405 nm laser wavelength and at a dose of 80 mJ/cm^2.
- Development of the photoresist in MF CD-26 for 80 s followed by rinsing in deionized (DI) water for 60 s.
- Deposition of 5 nm Cr and 15 nm Au using an electron-beam evaporator.
- Liftoff by soaking the wafer in N-methyl pyrrolidone (NMP) for 5 hours.
- Removal of excess PMGI by soaking the wafer in MF CD-26 for 30 s.
- Spin-coating of Microposit S1813 positive tone photoresist at 4 krpm for 60 s (thickness $\approx$ 1.8 **μ**m) and baking at 100°C for 90 s.
- Dicing of the 4" wafer into 1 $\times$ 1 cm^2 samples.
- Cleaning of the samples by sonication in acetone and isopropanol baths for 300 s each.
- Deposition of 10 nm WO_3 using ALD with Bis(tert-butylimino)bis(dimethylamino)tungsten (VI) (BTBMW) and O_3 precursors at 330°C.
- Plasma-Enhanced Chemical Vapor Deposition (PECVD) of 10 nm PSG using 1420 sccm N_2O, 12 sccm SiH_4, and 12 sccm PH_3 (2% in H_2) at 100°C, with a RF plasma power of 60 W at 380 kHz.
- Spin-coating of Microposit S1813 positive tone photoresist at 4 krpm for 60 s (thickness $\approx$ 1.8 **μ**m) and baking at 100°C for 90 s.
- Exposition of the active layer (**WO_3** and PSG channel pattern) layout using a Heidelberg-MLA 150 with a 405 nm laser wavelength and at a dose of 80 mJ/cm^2.
- Development of the photoresist in MF CD-26 for 60 s followed by rinsing in DI water for another 60 s.
- Patterning of both PSG and WO_3 layers using Reactive Ion Etching (RIE) with a CF_4 plasma at 100 W for 180 s (partitioned in 60 s intervals).
- Selective wet-etching (undercut) of the WO_3 layer in MF CD-26 for 300 s at room temperature.
- Stripping of the excess photoresist in N-methyl pyrrolidone (NMP) bath for 12 hours.

- Spin-coating of PMGI at 4 krpm for 60 s (thickness ≈ 120 nm) and baking at 180°C for 90 s. Spin-coating of Microposit S1813 positive tone photoresist at 4 krpm for 60 s (thickness ≈ 1.8 **μ**m) and baking at 100°C for 90 s.
- Exposition of the gate electrode layout (M2) using Heidelberg-MLA 150 with a 405 nm laser wavelength and at a dose of 80 mJ/cm^2.
- Development of the photoresist in MF CD-26 for 80 s followed by rinsing in DI water for another 60 s.
- Deposition of 5 nm Pd using an electron-beam evaporator at a low deposition rate (≤ 0.5 Å/s).
- Liftoff by soaking the pieces in NMP for 5 hours.
- Removal of the excess PMGI by soaking the pieces in MF CD-26 for 30 s
- Spin-coating of PMGI at 4 krpm for 60 s (thickness ≈ 120 nm) and baking at 180°C for 90 s. Spin-coating of Microposit S1813 positive tone photoresist at 4 krpm for 60 s (thickness ≈ 1.8 **μ**m) and baking at 100°C for 90 s.
- Exposition of the pad (M3) layout using Heidelberg-MLA 150 with a 405 nm laser wavelength and at a dose of 80 mJ/cm^2.
- Development of the photoresist in MF CD-26 for 80 s followed by rinsing in DI water for 60 s.
- Deposition of 10 nm Cr and 150 nm Au using an electron-beam evaporator.
- Liftoff by soaking the wafer in NMP for 5 hours.

The sheet resistance of the ALD WO_3 was ~18.2 kΩ/□ as deposited, which then slightly decreased to ~13.5 kΩ/□ during the fabrication process. On the other hand, the PSG layer we used in this work shows good electronic insulation properties. For example, for a device with 5 um width and 50 μm length, 3 V gate voltage yielded a current of ~200 pA (~15 GΩ), indicating that the electrolyte layer is much more resistive than the channel layer (R_{SD} ~ 1.4 MΩ).

Regarding the yield rate of this process, 130 devices were fabricated on a 1×1 cm^{2}chip. Out of the 50 devices we measured, 41 functioned successfully and reproducibly over the course of more than 2 months of experimentation.

Since we demonstrate standard Si fabrication compatibility, the fabrication flow can be easily adapted to yield nanoscale devices by simply replacing photolithography steps with electron-

beam lithography steps.

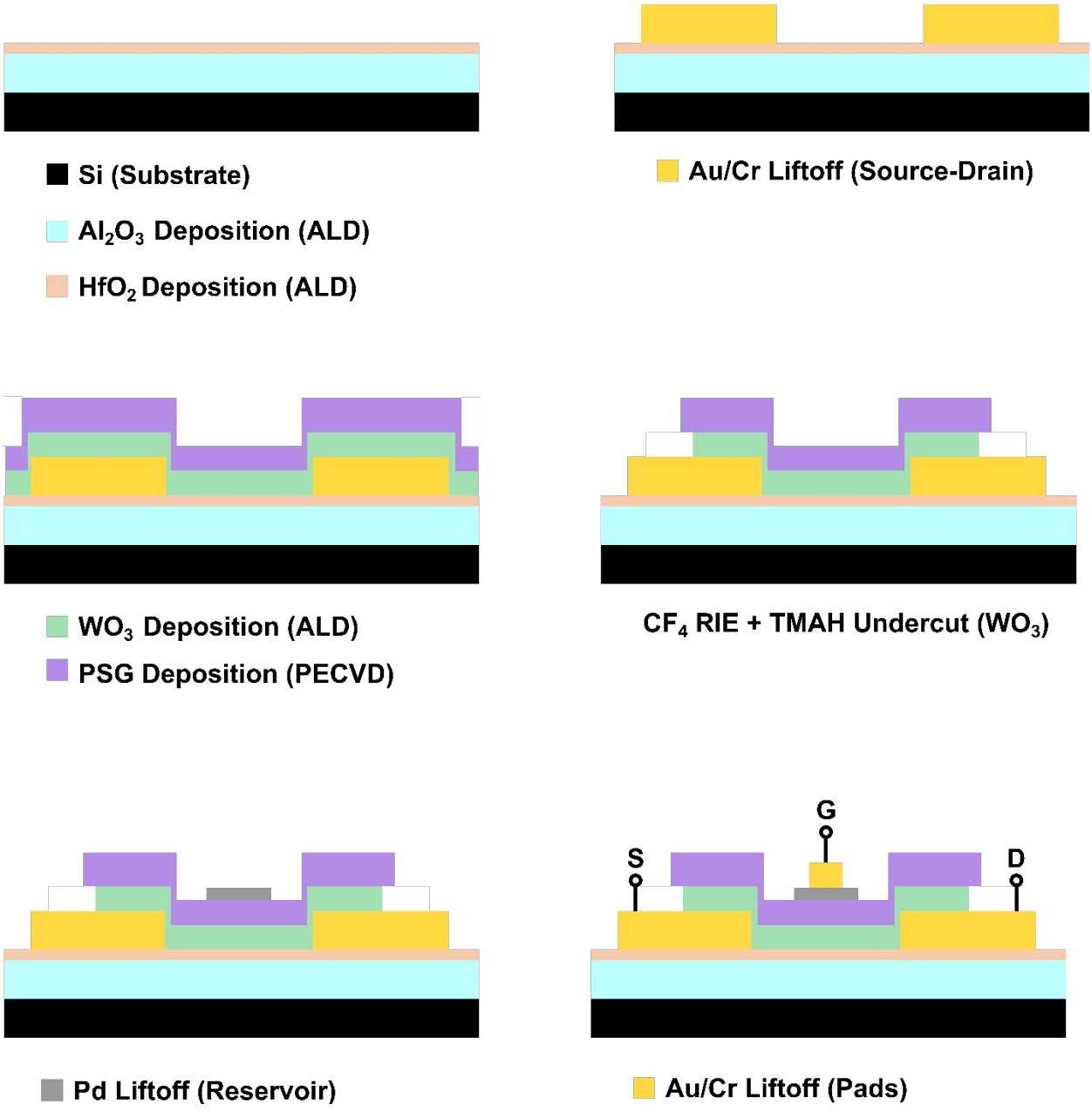


Figure S2. Fabrication flow of CMOS-compatible protonic nonvolatile resistors based on PSG electrolyte.

3. Methods

All electrical measurements were performed using a micro-probe station enclosed chamber (MPS-PT) manufactured by NEXTRON, Korea. In experiments performed in forming gas (FG, 3% H_2 in N_2) all 4 DC probes where first connected to the pads of the device under test (1 to Source, 1 to Drain and 2 to Gate terminals). The chamber was then purged by flowing in FG for 60 s with both gas inlet and outlet open, followed by another 60 s with outlet shut to create positive pressure inside the chamber.

Three of the probes (1 Source, 1 Drain and 1st Gate) were then connected to the Source Measurement Units (SMUs) of a Keysight B1500 Semiconductor Analyzer, while the fourth probe (2nd Gate) was connected to the Pulse Generation Unit (PGU) of the same instrument. The experiment sequence and data acquisition were controlled via an in-house developed MATLAB suite.

4. Additional Results

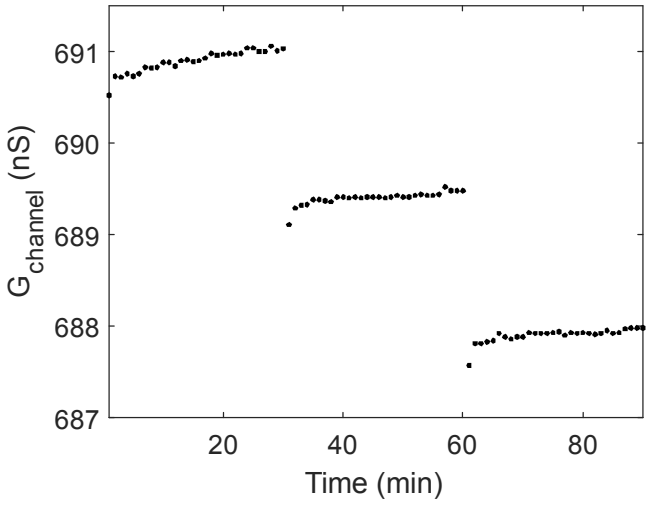


Figure S3. Retention characteristics of the protonic device incrementally programmed by a voltage pulse ($V_{pulse} = -4\ V, t_{pulse} = 1\ s$) at 30 and 60 minutes. Each conductance state is read every minute by sweeping V_{SD} between $\pm$ 0.1 V while the gate terminal is floating. Conductance of the device remains distinctly separate from adjacent levels over 30 minutes of readout.

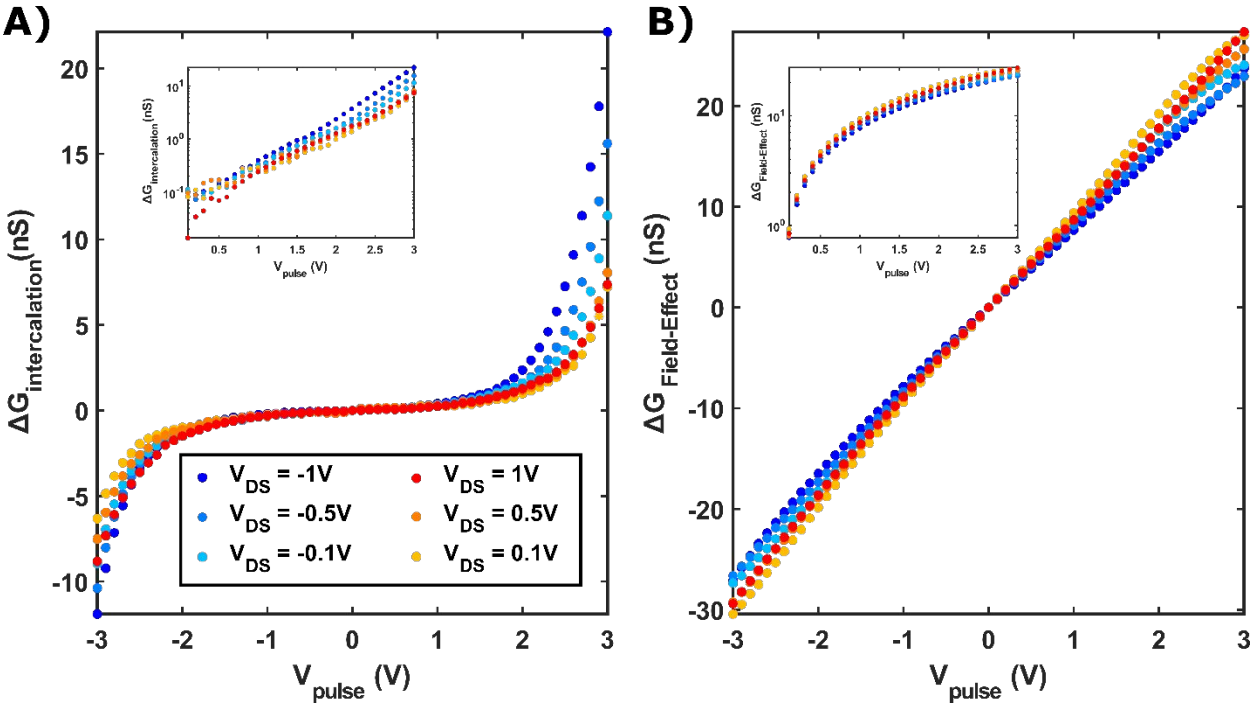


Figure S4. (A) Intercalation and (B) field-effect conductance modulation as a function of the pulse gate voltage for different read drain-source voltage.

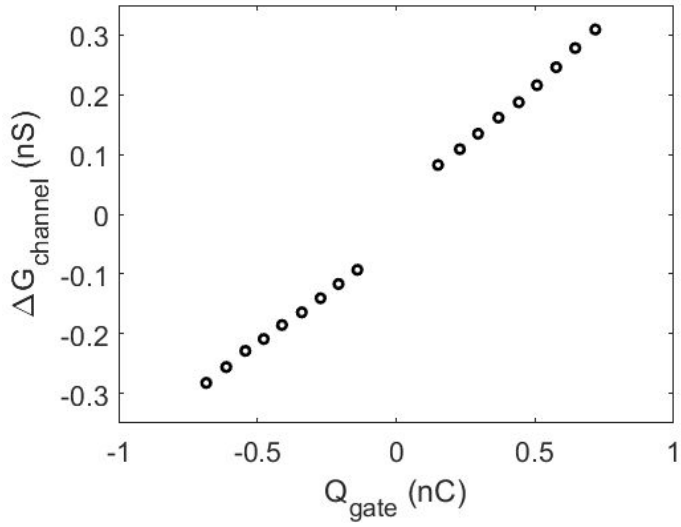


Figure S5. Linear dependence of change in channel conductance ($\Delta G_{channel}$) as a function of charge injected to / extracted from the gate (ΔQ_{gate}).

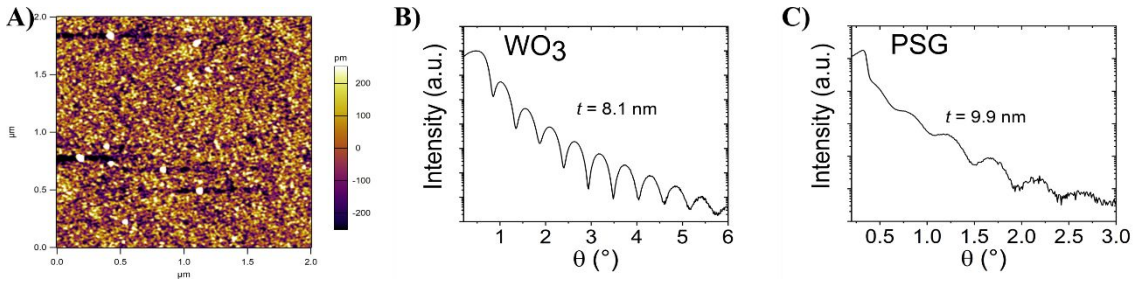


Figure S6. (A) Atomic force microscopy image of the reference ALD WO_3 thin film surface, deposited on a Si surface alongside the patterned sample. X-ray reflectivity (XRR) curve of the reference (B) ALD WO_3 and (C) PSG 12:12 thin films, deposited on a Si surface alongside the patterned samples.

The very smooth surface and low RSM roughness (≈ 0.2 nm) of the ALD WO_3 film as well as the presence of well-defined thickness-interference (Kiessig) fringes in the XRR curves of both WO_3 and PSG indicates that the films' surface is smooth and the film-substrate interface well defined. The film thickness (t) can thus be calculated from these XRR curves from the following equation $t = \frac{(m-n)\lambda}{2(sin\theta_m - sin\theta_n)}$

where m and n are the orders of interference, and θ_m and θ_n are the corresponding diffraction angles, respectively.

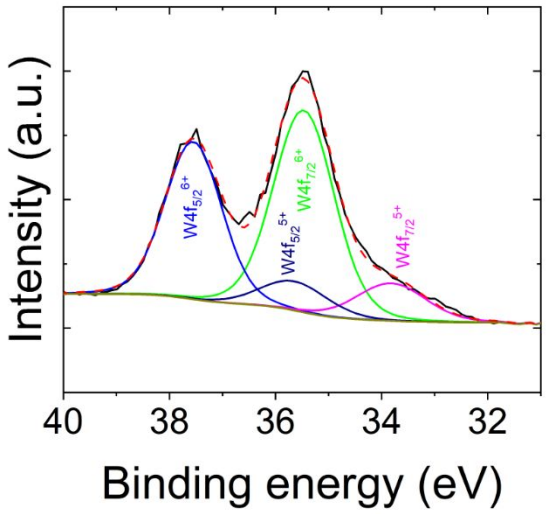


Figure S7. X-ray photoelectron spectra of the W 4*f* peak of a WO_3 thin film deposited by ALD. The W $4f_{5/2}$ and W $4f7_{/2}$ peaks deconvolution between the W^{6+} and W^{5+} oxidation states evidences a strong W^{5+} contribution (≈ 1 W^{5+} : 4 W^{6+} ratio), indicative of the initial reduced (substoichiometric, WO_{3-x}) nature of the film.

5. Additional Discussion

Unlike the P-concentration in PSG, we did not control the amount of H in Pd. From the pressure-concentration isotherms of the H/Pd system given by Lewis (Platinum Metals Rev., **4**, 132, 1960), the atomic ratio of H/Pd at room temperature and ambient pressure is ~0.65. Since we use premixed 3% H_2in N_2, we have only measured devices with this H/Pd ratio and assumed that the amount of H shuffled in/out of the WO_3 channel is much less than the amount of H stored in the reservoir. There are two reasons behind running the experiments under forming gas environment. (1) Under storage conditions (N_2) prior to experimentation, Pd has no H within. The hydrogenation occurs when the device is enclosed in a forming gas ambient. (2) For Pd to retain H, it should not be exposed to O_2, which causes hydrogen to oxidize and leave the reservoir material. Once the reservoir is loaded with H, it can alternatively be operated under an inert environment (e.g. N_2, Ar, vacuum) as well.

We want to note that in measurements performed on devices with thicker Pd layers (~ 80 nm), we observed that the H uptake caused volume expansion of the Pd layer to the extent of it getting exfoliated. We anticipate that higher H_2 concentration could therefore be problematic even for devices with thinner Pd layers. On the other hand, as the number of protons that are exchanged with the channel layer is much less than what is stored in the reservoir, we expect that devices would be operational under lower H_2 concentrations as well.